What is claimed is:

1. An apparatus for testing at least one first integrated circuit (IC) and at least one second IC, comprising:

a first tester adapted to test the at least one first IC with a first test procedure;

a second tester adapted to test the at least one first IC with a second test procedure simultaneously while the first tester tests the at least one second IC with the first test procedure; and

a single handler coupled to the first and second testers; wherein the first and second test procedures are adapted to test at least some different IC parameters.

2. The apparatus according to Claim 1, wherein a portion of the second test procedure comprises the same IC tests as at least a portion of the first test procedure.

3. The apparatus according to Claim 1, further comprising:

a first test head coupled to the first tester;

a first load board coupled to the first test head and the handler;

a second test head coupled to the second tester; and

a second load board coupled to the second test head and the handler.

4. The apparatus according to Claim 3, further comprising:

a first device adapted to move the first IC's to the first load board; and

a second device adapted to move the second IC's to the first load board simultaneously while the first device moves the first IC's to the second load board.

5. The apparatus according to Claim 1, wherein the first tester is a low cost tester and the second tester is a high cost tester, wherein the first test procedure is completed by the completion of the second test procedure.

6. The apparatus according to Claim 1, wherein the apparatus is adapted to move the at least one first IC to the second tester simultaneously while the apparatus moves the at least one second IC to the first tester.

7. The apparatus according to Claim 6, wherein the apparatus is adapted to move the at least one second IC to the second tester, simultaneously while moving at least one third IC to the first tester.

8. The apparatus according to Claim 1, wherein the first test procedure comprises prescreening tests, wherein the second test procedure comprises detailed functional tests.

9. The apparatus according to Claim 1, further comprising at least one third tester coupled to the handler adapted to test the first IC's with a third test procedure while simultaneously testing the second IC's.

10. The apparatus according to Claim 1, wherein first IC's that fail the first test procedures are not moved to the second tester for testing with the second test procedure.

11. The apparatus according to Claim 1, wherein the first and second IC's are packaged.

12. A method of testing at least one first integrated circuit (IC) and at least one second IC in an apparatus comprising a first tester and a second tester coupled to a single handler, the method comprising:

testing the first IC with a first test procedure using the first tester; and

testing the second IC with the first test procedure simultaneously while testing the first IC's with a second test procedure using the second tester, wherein testing IC's with the first test procedure comprises testing at least some different IC parameters than testing IC's with the second test procedure.

13. The method according to Claim 12, wherein the first tester is a low cost tester and the second tester is a high cost tester, further comprising:

completing the first test procedure by the completion of the second test procedure.

14. The method according to Claim 12, further comprising moving the first IC's to the second tester simultaneously while moving the second IC's to the first tester.

15. The method according to Claim 12, wherein the first test procedure comprises testing IC's with prescreening tests, wherein the second test procedure comprises testing IC's with detailed functional tests.

16. The method according to Claim 12, wherein the apparatus includes at least one third tester coupled to the handler adapted to test the first IC's with a third test procedure simultaneously while testing the second IC's.

17. The method according to Claim 12, further comprising not moving first IC's that fail the first test procedures to the second tester for testing with the second test procedure.

18. The method according to Claim 12, wherein the first and second IC's are packaged.

19. A method of testing integrated circuits (IC's), comprising:

providing at least one first IC;

providing at least one second IC;

testing the at least one first IC with a first test procedure; and

testing the at least one first IC with a second test procedure simultaneously while testing the at least one second IC with the first test procedure, wherein the first and second test procedures are performed within a single enclosed handler, wherein testing IC's with the first test procedure comprises testing at least some different IC parameters than testing IC's with the second test procedure.

20. The method according to Claim 19, wherein the first tester comprises a low cost tester, wherein the first test procedure comprises testing IC's with prescreening tests, wherein the second tester comprises a high cost tester, and wherein the second test procedure comprises testing IC's with detailed functional tests.